Remarks

The final Office Action dated October 29, 2008 notes an objection to claim 1 due to informalities and that claims 1-20 stand rejected under 35 U.S.C. § 103(a) over Hennessy ("Computer Organization and Design: The Hardware/Software Interface") in view of Colwell (U.S. Patent No. 5,604,878). Applicant traverses the rejection and, unless explicitly stated by the Applicant, does not acquiesce to any objection, rejection or averment made in the Office Action.

Applicant has amended claim 1 consistent with the suggestion of the Office Action of October 29, 2008. Applicant requests that the objection be removed.

Applicant respectfully traverses the rejection under 35 U.S.C. § 103(a) over Hennessy in view of Colwell. Applicant respectfully submits that, among other things, the rejection fails because there is not correspondence to each limitation; the references teach away from any combination that conforms to the claim limitations; the Office Action relies upon mischaracterizations of the teachings of the references; the alleged reason(s) for the modifications are illogical and unsupported, and the proposed combination would not achieve the asserted benefits.

The Office Action does not show correspondence to each limitation including those limitations directed to the latch being located between two pipeline stages and to the enable signal being overridden by the control signal. A claimed invention is not rendered obvious simply because the elements of the invention are independently found in the prior art. Indeed, most, if not all, inventions are made from elements that were in some sense known. Thus, where no single reference teaches each limitation there must be a clearly articulated reason for the combination. In presenting an obviousness rejection it is important to consider differences between the teachings, including those teachings that would lead the skilled artisan away from the proposed combination. *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007)

The Hennessy and Colwell references fail to teach each element of the claims including those limitations directed towards a latch between two pipeline stages and overriding of an enable signal by a control signal. The rejection relies upon the teachings of Colwell to cure deficiencies of the Hennessy reference. The relied upon portions of

Colwell, however, are implemented in connection with an extension buffer 60 and multiplexor 61. These components are extensions to the pipeline 31 to delay, if necessary, the final output of the pipeline. *See,* Colwell at Col. 7, line 37 *et seq*. To the extent that Colwell teaches multiple modes of storage/truncated pipelines, Colwell teaches that the memory element (buffer 60) is placed at the end of the final pipeline stage. *See,* Colwell at FIG. 3. Moreover, it does not make sense to place the extension mechanism in any other location because the stated purpose of these components is to delay the output of the pipeline for a clock cycle. As such, were the skilled artisan to implement the teachings of Colwell into the pipeline stage of Hennessy, the teachings would be implemented in a manner that would not conform to the claim limitations directed to the latching being located between two pipeline stages.

Moreover, the Office Action has misinterpreted the teachings of at least the Colwell reference with regards to overriding of an enable signal and thereby fails to show correspondence to related limitations. The Office Action equates a clock signal (incorrectly identified as inherent)[1] to an enable signal. In no manner, however, does Colwell teach that such an enable signal is overridden by the control signal. Instead, Colwell teaches that the control signal controls multiplexor 61 to selectively provide either the input of buffer 60 or the output of buffer 60. Thus, the control signal does not change the functionality of buffer 60 because, regardless of the control signal, data is still saved in buffer 60. For example, if the output of pipeline stage 3 has a value "A", this value A is passed to both buffer 60 and multiplexor 61. Multiplexor 61 responds to the control signal by sending value A to bus 120 either immediately or after being stored in buffer 60; however, the value A is still stored in buffer 60 regardless of the control signal. Thus, the enable signal is not overridden by the control signal. Notwithstanding, Applicant has made amendments to further clarify that, when the enable signal is overridden, the data is passed through the latch independent of the enable signal. Accordingly, Applicant respectfully requests that the rejections be withdrawn.

[1] Applicant notes that clock signals are not inherent to laches as many laches do not use a clock signal (see, e.g., Applicant's specification FIG.3, latch 28, see also M.P.E.P. 2112).

Applicant further submits that the teachings of the Hennessy and Colwell references would lead the skilled artisan away from any combination that corresponds to the claim limitations. In *KSR,* the Supreme Court looked favorably on *Adam's* treatment of teaching away stating, "when the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious." The Court further tied in the relationship between the teach-away standard and demonstrating unpredictable results. "The fact that the elements [in *Adams*] worked together in an unexpected and fruitful manner supported the conclusion that Adam's design was not obvious to those skilled in the art." *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007).

The Office Action's asserted combination includes a modification of the pipeline shown in FIG. 6.32 of Hennessy. The modification includes adding the pipe extend buffer 60 and MUX 61 of Colwell. As taught by Colwell, the pipe extend buffer 60 and MUX 61 are implemented to address concerns related to contention of execution units that share a common write-back port. *See, e.g.*, Colwell Col. 2, lines 60-63. There is no evidence that the pipeline of Hennessy suffers from such contention. Moreover, adding the additional pipe extend buffer 60 only serves to delay execution times of the pipeline, thereby avoiding contention with another pipeline. Thus, the skilled artisan would not look to the teachings of Hennessy and Colwell references to implement a delay the pipeline of Hennessy that addresses a nonexistent contention problem and only serves to slow the pipeline processing. As such, the references teach away from the asserted combination and the combination is not obvious.

Moreover, the alleged reason(s) for the modifications are illogical and unsupported in part because the proposed combination would not achieve the asserted benefits. To establish an obviousness rejection there must be a clearly articulated reason for the combination/modification because claimed discoveries almost of necessity will be combinations of what, in some sense, is already known. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398 (U.S. 2007). The reason for the proposed modification is to obtain the "advantage of bypassing an extra pipeline stage that isn't needed for instructions". *See,* Instant Office Action at page 5. The proposed modification, however, does not bypass an "extra pipeline stage." Rather, as discussed above, Colwell teaches that the purpose of

the pipe extend buffer 60 and MUX 61 is to effectively delay the pipeline. As such, the reason presented for the modification is based upon an incorrect interpretation of how the combination would function (*e.g.*, incorrectly asserting increased speed when the combination would decrease speed). Thus, the modification would not achieve the stated benefit of bypassing a pipeline stage. As there is no remaining reason to implement the modification/combination, Applicant respectfully submits that the obviousness rejection cannot stand and requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Aaron Waxler, of NXP Corporation at (408) 474-9068 (or the undersigned).

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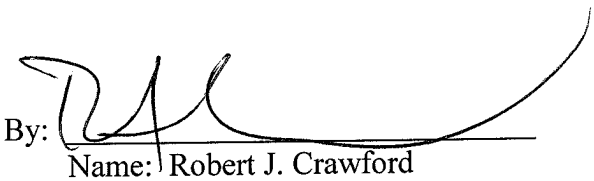
By: 

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